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Question Paper Code : 81240

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2025.

Fifth Semester

Electronics and Communication Engineering

EC 3552 — VLSI AND CHIP DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Differentiate between NMOS and CMOS logic families.
2. Define static and dynamic power consumption in MOS devices.
3. Define Elmore's constant and state its importance.
4. What is a stick diagram?
5. Define setup time and hold time for latches.
6. Distinguish between static and dynamic registers.
7. Define memory core and memory peripheral circuitry.
8. List the interconnect parameters that influence signal delay.
9. What is scan design in testability?
10. Mention the purpose of Automatic Test Pattern Generation.

PART B — ($5 \times 13 = 65$ marks)

11. (a) Explain the static and dynamic behavior of a CMOS inverter with necessary waveforms.

Or

- (b) Draw and explain the I-V characteristics of MOSFET under ideal and non-ideal conditions.

12. (a) With a neat layout, design a 2-input NAND gate using CMOS technology and explain the layout steps.

Or

- (b) Discuss the delay modeling of CMOS logic using Elmore delay estimation.
13. (a) Explain the working and design of static latches and registers using CMOS Inverters.

Or

- (b) Describe the timing classification of digital systems with suitable timing diagrams.
14. (a) Discuss how FPGAs are used for logic implementation and rapid prototyping.

Or

- (b) Design a 4-bit ripple carry adder and explain its working at the transistor level.
15. (a) Describe various fault models used in digital testing and their detection mechanisms.

Or

- (b) Discuss the test and verification challenges in SOC (System on Chip) designs.

PART C — (1 × 15 = 15 marks)

16. (a) Design a 4-bit combinational adder using pass-transistor logic that meets low power and area constraints.
- (i) Show transistor-level schematic,
 - (ii) Estimate propagation delay using Elmore's constant, and
 - (iii) Propose optimization steps to enhance performance.

Or

- (b) Design a two-stage pipeline register system for high-speed data transfer in a synchronous digital system operating at 500 MHz.
- (i) Identify timing constraints (setup/hold, skew, jitter, Optimize clocking strategy,
 - (ii) Interpret timing diagrams.